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(54) Integrated circuit subsurface breakdown diode structure and process

(57) A subsurface avalanche or Zener diode (20) formed in a conventional bi-polar integrated circuit structure (10) includes a P type substrate (5), an N type epitaxial "collector" region (3A) surrounded by a deep P+ type "isolation" region (1) extending from the surface of the structure to the P type substrate, a relatively lightly doped P type "base" region (18) disposed in the N type "collector" region, a relatively heavily doped N+ type "emitter" region (27) disposed within the P type "base" region, and a heavily doped implanted P+ type region (19'') disposed immediately beneath and contiguous with a central portion of the N+ type "emitter" region. This P+ type region does not extend to the P type substrate (5). A peripheral portion (27') of the N+ type "emitter" region laterally subtends the implanted P+ type region. The disclosed structure provides a very stable, very low voltage avalanche or zener junction that confines avalanche or zener operation to the subsurface junction between the implanted P+ type region and the portion of the N+ type "emitter" region contiguous therewith.

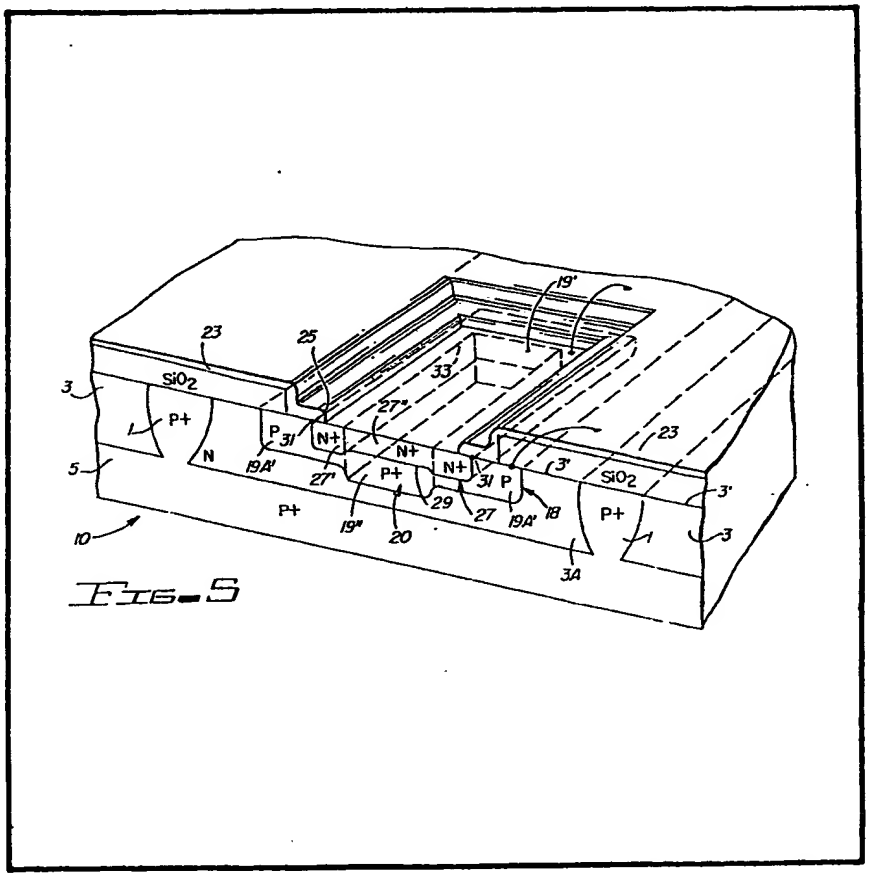

Fig-5

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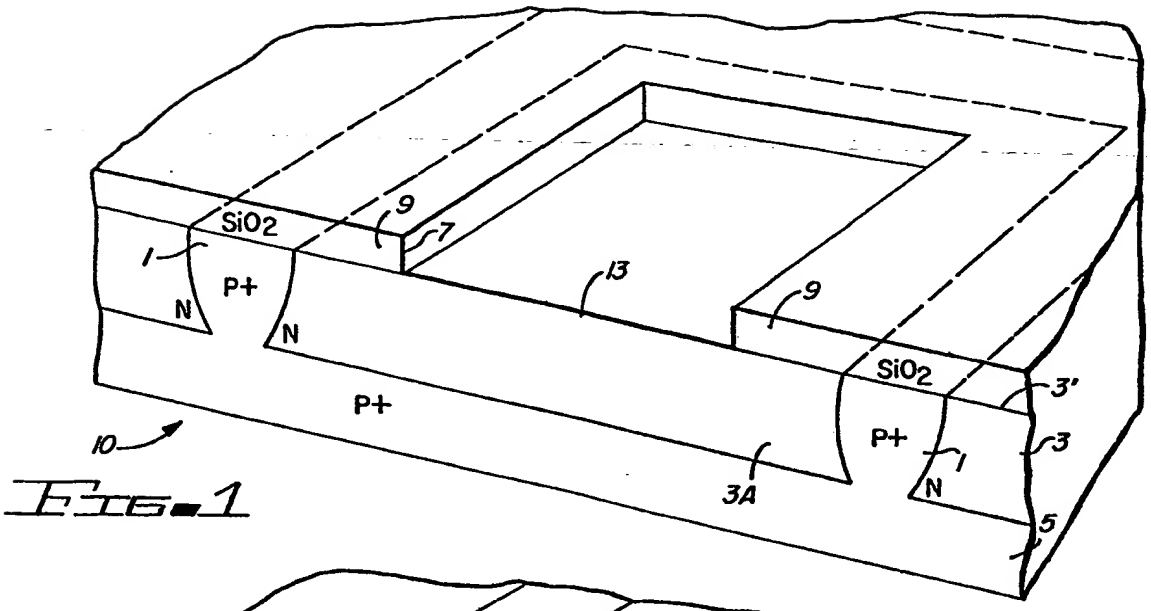

FIG. 1

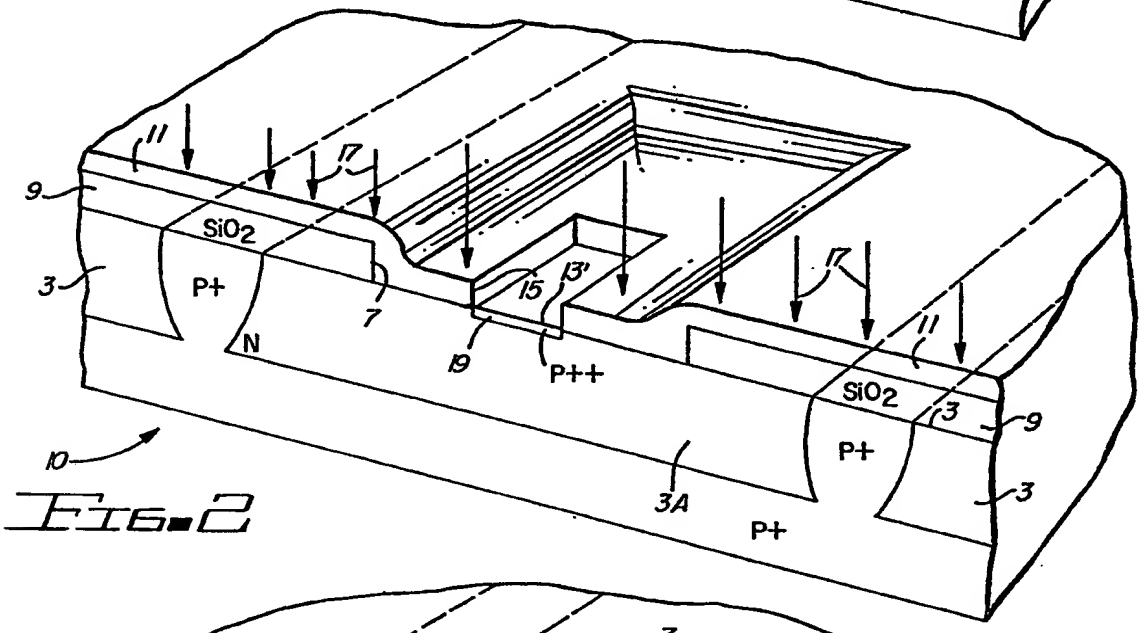

FIG. 2

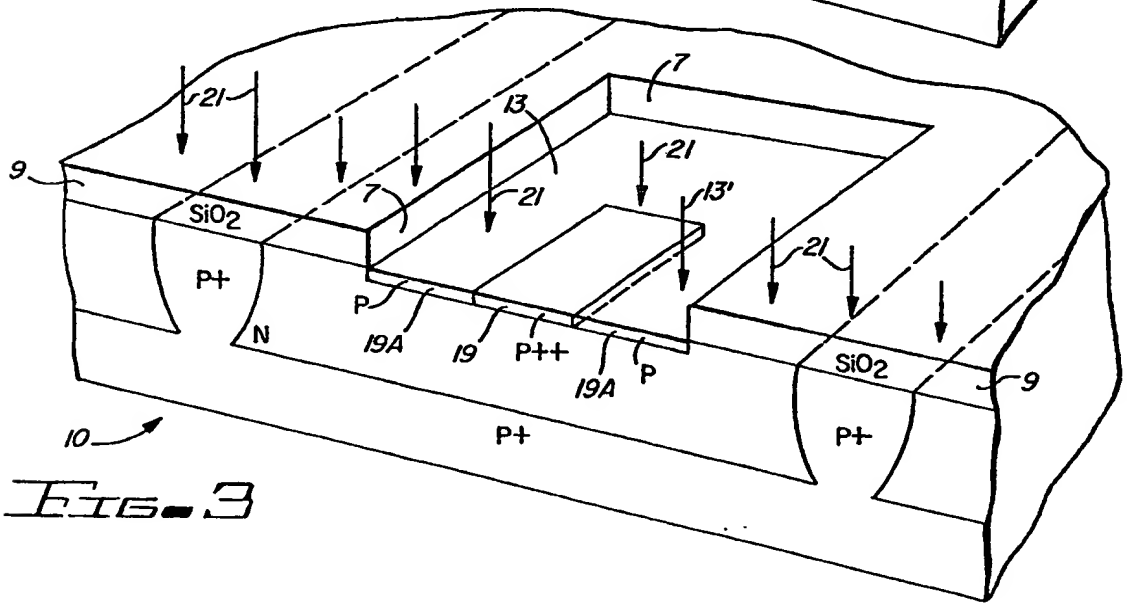

FIG. 3

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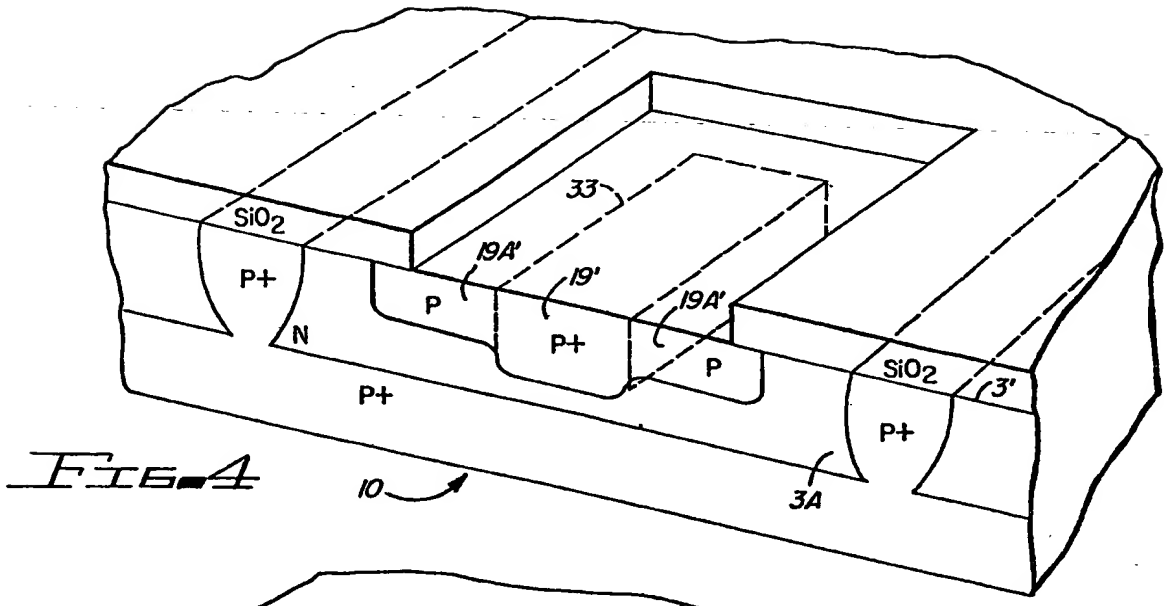

FIG-4

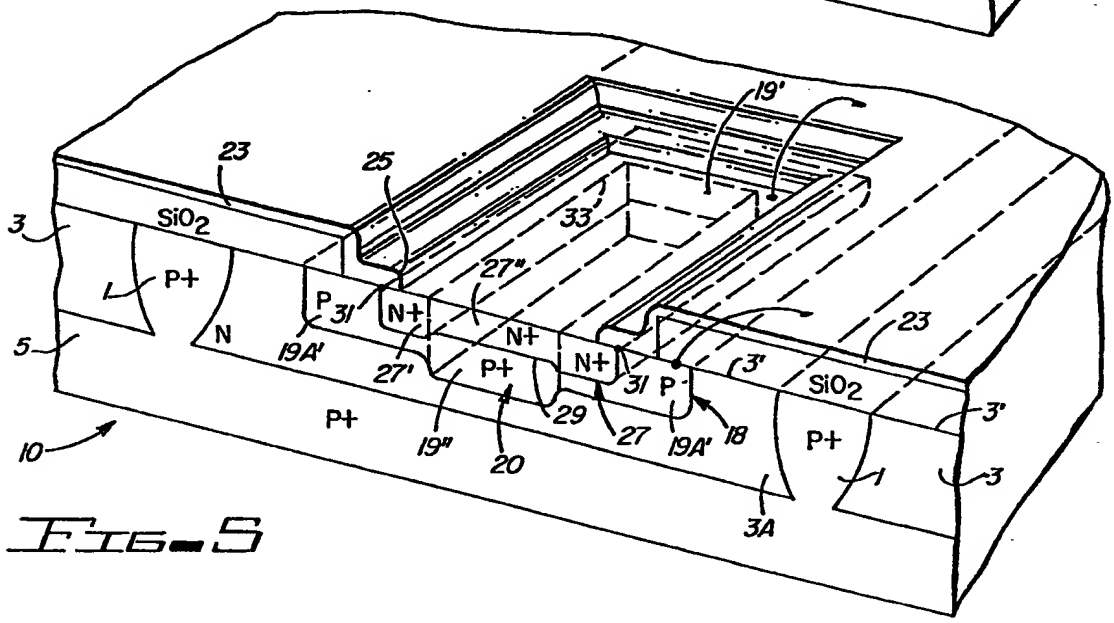

FIG-5

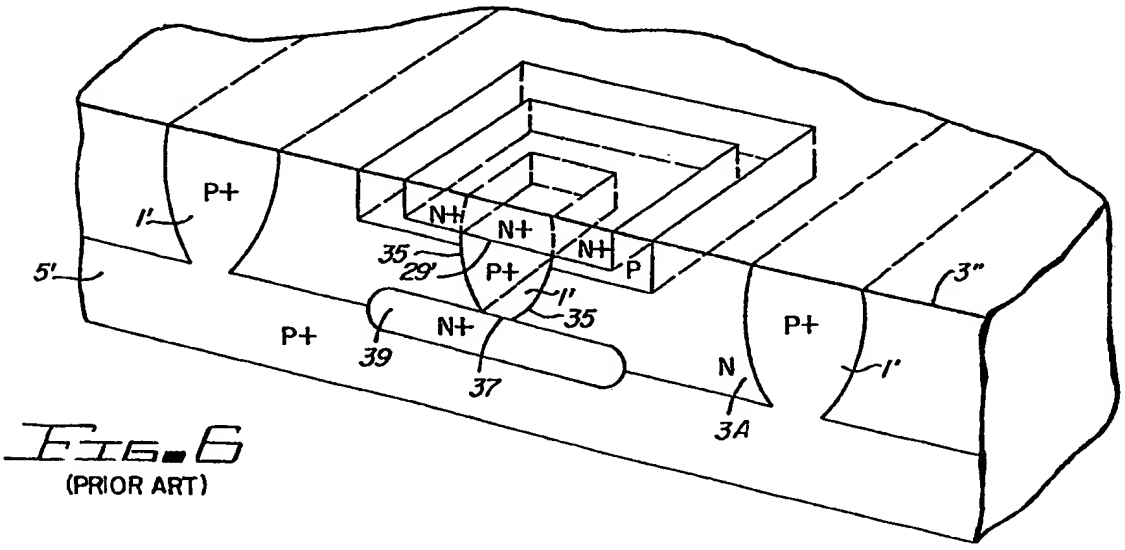

FIG-6
(PRIOR ART)

SPECIFICATION

Subsurface breakdown diode structure

The present invention relates to avalanche diode structures having subsurface avalanche junctions, and more particularly to subsurface avalanche and zener junction structures which have low parasitic capacitance and which provide very low avalanche or zener voltages without concomitant high leakage currents that result from dislocations caused during diffusion of heavily doped regions.

A great need exists in the monolithic integrated circuit art (and also the hybrid integrated circuit art) for highly stable, low noise, avalanche and zener diodes having very low avalanche voltages. Such highly accurate avalanche or zener diodes are used as voltage references in a variety of precision monolithic integrated circuits and also in hybrid integrated circuits, especially in analog devices such as digital to analog converters, analog to digital converters, voltage to frequency converters, certain kinds of switching devices, and also in various digital circuits.

At this point, it should be pointed out that the terms "avalanche" and "zener" often are interchangeably used in the art, the term "zener" being more commonly used to refer to all kinds of PN junction reverse breakdown mechanisms, even though technically, zener breakdown is a quantum mechanical tunnelling phenomena, rather than an avalanche breakdown phenomena. Herein, the term "avalanche" will be used to encompass both, since the particular breakdown mechanism occurring is irrelevant to the structure of the present invention.

Unfortunately, it has been difficult to obtain the high degree of stability and low noise needed in avalanche diodes, at least not without introducing excessive cost and complexity to the integrated circuit manufacturing processes. It is well known that so-called "surface phenomena" due to various types of impurities and/or crystal defects at or near the oxide-silicon interface in conventional monolithic integrated circuit devices often cause undesirable instability (with respect to temperature and/or time) and also cause avalanche noise in avalanche diodes of the type in which the avalanching phenomena occurs at or very close to the oxide-silicon interface. In order to overcome this instability and noise, various integrated circuit device structures have been proposed to provide subsurface junctions in which the avalanching (or zener) phenoma is confined to junction areas that do not terminate at or near the oxide-silicon interface region. For example, U.S. Patents No. 4,213,806; No. 4,127,859; No. 4,109,169; No. 4,106,048; No. 4,106,043 and No. 4,203,781 are believed to be generally representative of the state of the art. However, none of the devices disclosed in any of the above references is really ideal for use in conjunction with a "conventional" integrated circuit manufacturing process if the doping levels are selected so as to provide what would be considered to be a really "low" reverse voltage across the avalanching buried junction i.e. a voltage less than approximately seven volts.

For example, in the device disclosed in Patent No. 4,213,806, if the doping level of the base region is relatively high, so as to provide a sheet resistance of roughly 150 ohms per square (for a junction depth of approximately 2.5 microns), and if the depth of the "collector" region is roughly 15 microns (in order to provide BV_{CEO} voltages of the order of 40 volts), then the surface concentration of the boron dopant (which is what is commonly used) for the isolation regions must be nearly 10^{20} atoms per cubic centimeter in order to confine the avalanche mechanism to the subsurface N+P+ junction described in U.S. Patent No. 4,213,806. In that patent, the subsurface avalanche junction is provided by diffusing a particular heavily doped P+ region at the desired location of the buried junction at the same time that the P+ isolation diffusions are made to isolate the various collector regions in the integrated circuit. The base region is subsequently formed by conventional diffusion processes so that it completely surrounds the upper portion of that particular heavily doped P+ region, which extends all the way from the silicon surface to a conventional underlying N+ "buried layer". An N+ emitter region is then formed within that particular heavily doped P+ region at the same time that emitters are diffused for transistors elsewhere in the subject integrated circuit.

The above described structure of US Patent No. 4,213,806 has numerous shortcomings. Conventional boron diffusion processes have long been known to cause severe "pitting" of the exposed silicon surface, and also cause other surface damage, including inducing surface dislocations, if the surface concentration is of the order of 10^{20} atoms per cubic centimeter. Such surface damage and dislocations typically propagate deep into the silicon during subsequent high temperature diffusion "drive in" processes for the P+ isolation regions and also during the "base" and "emitter" diffusions. The result of such defects deep in the silicon crystal structure is that the diodes formed have "leaky" or "soft" junctions which may deleteriously affect circuit performance. Even for somewhat more lightly doped base regions, for which the surface concentration of the P+ "isolation" diffusion can be lowered somewhat while still causing the avalanching to be constrained to subsurface regions, the trade-off between the deleterious effects of surface damage caused by the P+ boron diffusions and the stability and quality of the subsurface diode is quite difficult.

In addition to the marginal quality of the subsurface avalanche diode devices obtainable using the structure and process disclosed in U.S. Patent No. 4,213,806, that structure inherently has the further shortcoming that the "sidewall" capacitance associated with the portion of the P+ region extending from the bottom of the base region of the subsurface diode to the N+ "buried

layer" and the capacitance of the junction between the bottom of the P+ region and the top of N+ buried layer region both are quite high. These two parasitic capacitances are in parallel with, and therefore add to, the junction capacitance of the subsurface avalanching N+P+ junction between the bottom of the N+ emitter diffusion region and the top of the P+ diffusion region. This total parasitic capacitance is more than double the junction capacitance of the avalanching junction itself.

Although the total capacitance associated with the avalanching junction is not important in some circuit applications of avalanche junctions when they are used as voltage references within integrated circuits, this parasitic capacitance is very important in other applications. For example, there is a common operational amplifier circuit in which resistance feedback from the output of the operational amplifier to one input thereof is limited by an avalanche diode connected in parallel with the feedback resistor. The other input of the operational amplifier is grounded, so the output of the operational amplifier rises linearly until the voltage across the feedback resistor increases to the point where the avalanche diode breaks down. Thereafter, the output of the operational amplifier is equal to the avalanche voltage. Obviously, any additional parasitic capacitance of the avalanche diode decreases the bandwidth of this device, and thus impairs its high frequency response.

Furthermore, since the junction area along the above-mentioned sidewall of the subject P+ region and the junction areas along the P+N+ buried layer to P+ region interface represent parasitic diodes connected in parallel with the desired low voltage, highly stable avalanche diode, any "softness" or leakage in these parasitic junctions caused by propagated silicon defects resulting from the damage due to the heavy P+ boron diffusion can impair the stability and low noise properties of the desired avalanche diode.

In short, even though the teaching of U.S. Patent No. 4,213,806 is that the disclosed subsurface avalanche diode avoids the problems encountered with typical "surface breakdown" diodes, and achieves this without introducing additional cost into the conventional integrated circuit manufacturing process, the fact is that the overall quality of that subsurface avalanche diode is poor. Furthermore, since in a conventional integrated circuit manufacturing process, the P+ "isolation" diffusion is not considered to be a "critical" step, ordinarily relatively little process control over the isolation diffusion step of the process is required, reducing the overall cost of the conventional manufacturing process. However, it is recognized in U.S. Patent No. 4,213,806 that very close control over the P+ "isolation" diffusion needed in that structure is required if the desired subsurface avalanching junction is to be obtained. Thus, there is a "hidden" cost, in the form of close control of a formerly loosely controlled process step, that must be added to the costs of the conventional integrated circuit manufacturing process if the structure and process of U.S. Patent No. 4,213,806 are to be successfully used.

Despite the foregoing shortcomings of that subsurface avalanche diode structure and process they probably are the ones most commonly used today, simply because no other practical structure has been proposed. For example, the subsurface avalanche diode structures shown in U.S. Patent No. 4,127,859 suffer from precisely the same shortcomings as those disclosed in U.S. Patent No. 4,213,806 because the P type side of the subsurface avalanche diode is obtained by a P+ region formed during the heavily doped, damage causing "isolation" diffusion process.

Reportedly, a device has been proposed in which a subsurface avalanche junction structure has been provided by ion implanting a heavily doped P type region at the end of a conventional bipolar integrated circuit manufacturing process, wherein the ion implantation energies are such that the resulting heavily doped P type region is positioned beneath and abutting the previously formed "emitter" N+ region. However, this process is impractical for several reasons. First, in order to eliminate surface damage and "amorphousness" in the surface silicon produced by the implantation, and also in order to "activate" the implanted boron atoms by causing them to attain substitutional sites in the silicon lattice structure, a lengthy, high temperature annealing process must be carried out. This annealing process inherently "drives in" the previously formed PN junctions and also lowers the impurity concentrations immediately on either side of each PN junction, thereby increasing the minimum breakdown voltage that can be attained. Furthermore, use of this technique would require a major modification to the diffusion process in order to obtain bi-polar transistor characteristics that would be satisfactorily close to those associated with the original bipolar integrated circuit manufacturing process. As those skilled in the art will readily recognize, it is not a particularly easy matter to arrive at a completely satisfactory bi-polar integrated circuit manufacturing process, and once one is achieved, it is very undesirable to have to make significant modifications to it.

Thus, there remains an unmet need for a highly stable subsurface avalanche junction diode structure and a manufacturing process which is highly compatible with conventional bipolar integrated circuit manufacturing processes and which produces relatively low voltage, low noise avalanche or zener diodes having minimum parasitic capacitances.

Accordingly, it is an object of the present invention to provide an improved subsurface breakdown diode which is highly compatible with conventional bipolar integrated circuit manufacturing processes.

It is another object of the invention to provide an improved subsurface integrated circuit

avalanche or zener diode having a very low avalanche or zener breakdown voltage wherein the manufacturing process does not produce an unacceptably large amount of subsurface damage and/or dislocations in the silicon of the final integrated circuit.

It is another object of an embodiment of the invention to provide the lowest possible avalanche or zener breakdown voltage in a subsurface diode made by means of a conventional bipolar integrated circuit manufacturing process including forming of a P type substrate, an N type epitaxial "collector" region, a P+ "isolation" diffusion, a relatively lightly doped P type "base" region and a relatively heavily doped N+ type "emitter" region.

It is another object of the invention to provide a subsurface avalanche or zener diode structure and process for its production in a conventional bipolar integrated circuit structure wherein very little alteration of pre-existing processing procedures is required and wherein important device characteristics of transistors and diodes elsewhere in the integrated circuit are substantially unaffected.

It is another object of an embodiment of the invention to provide an integrated circuit subsurface avalanche or zener diode structure and process for its production which results in low parasitic capacitance and junction current being associated with the subsurface diode.

According to the present invention there is provided a low voltage integrated circuit subsurface avalanche or zener diode comprising in combination:

a P type substrate having a first surface;

an N type layer on said first surface, said N type layer having an outer surface;

a P+ isolation region extending from said outer surface through said N type layer to said P type substrate to isolate electrically a first N type region of said N type layer from any other portion thereof;

a P type region disposed in said first N-type region, the junction between said P type region and said N type region terminating at said outer surface;

a heavily doped N+ region disposed in said P type region the junction between said P type region and said N+ region terminating at said outer surface, and

an entirely subsurface P+ region continuous with and laterally surrounded by said P type region and disposed beneath and contiguous with said N+ region and forming a subsurface P+N+ junction therewith;

the majority carrier impurity concentration on each side of said subsurface P+N+ junction greatly exceeding the P type impurity concentration at any point along the boundary between said P type region and the peripheral portion of said N+ region.

According to a further aspect of the present invention there is provided a process for making a low voltage integrated circuit subsurface avalanche or zener diode, said method comprising the steps of:

(a) forming a first opening in a first oxide layer on the surface of a semiconductor chip which includes a P type substrate and a plurality of electrically isolated N type regions disposed on said substrate, a plurality of P+ isolation regions extending from outer surfaces of said N type regions to said P type substrate, said first oxide layer being disposed on said outer surfaces, said first opening exposing a first area of the surface of a first one of said N type regions;

(b) exposing a second area of the surface of said first N type region, the boundary of said second area being spaced from and disposed entirely within the boundary of said first area;

(c) passing P type impurities through said second opening into the exposed second area of the surface of said first N type region to form a shallow heavily doped P+ type first region that is coextensive with said second opening;

(d) passing P type impurities through said first opening to form a shallow P type second region surrounding and contiguous with said first region, said first region being substantially more heavily doped than said second region;

(e) heating said chip to diffuse said first and second regions deeper into said first N type region;

(f) forming a second oxide layer covering said first surface area and forming a third opening in said second oxide layer exposing a third area of the surface of said first N type region, the boundary of said third area being everywhere spaced from and disposed between the boundaries of said first and second areas;

(g) passing N type impurities through said third opening to form an N+ region in the exposed portions of said first region and said P type second region,

said N+ region having an inner portion approximately laterally co-extensive with said first region and a depth that is less than the depth of said first region, the bottom portion of said first region remaining P+ type, said N+ region also having a peripheral portion having an inner boundary that is essentially coterminous with an outer boundary of the junction between said P+ bottom portion of said first region, and said inner portion of said N+ region and said P+ bottom portion of said first region forming a P+N+ subsurface junction therebetween, the majority carrier impurity concentrations on each side of said P+N+ subsurface junction greatly exceeding the P type impurity concentration along the junction between said second region and said peripheral portion of said N+ region, thereby confining avalanching or zener tunnelling of the diode formed by said N+ region and said first and second regions to the vicinity of said P+N+ subsurface junction.

Briefly described, one embodiment of the present invention provides a highly stable low voltage integrated circuit subsurface avalanche or zener diode structure and a method of making it,

the structure including a lightly doped P type substrate, a relatively lightly doped N type layer separated into electrically isolated regions by a plurality of deep, heavily doped P+ isolation regions that extend from the top surface of the N type layer to the P type substrate, a P type "base" region disposed in a first one of the isolated N type regions and extending to the top surface thereof, a heavily doped N+ "emitter" region disposed in the P type "base" region and extending to the top surface thereof, and a heavily doped P+ subsurface region disposed in the P type "base" region beneath and contiguous with the N+ type "emitter" region and completely subtended thereby, so that an entirely subsurface P+N+ junction exists between the P+ subsurface region and the N+ "emitter" region, but does not extend to the P type substrate. The portion of the N+ type "emitter" region that is laterally coextensive with the P+ subsurface region has a lower net N type doping level than the peripheral portion of the N+ "emitter" region. The majority carrier impurity concentrations on either side of the P+N+ junction are substantially higher than the majority carrier impurity concentration in the P type "base" region, thereby confining avalanche or zener breakdown in the diode formed by the N+ type "emitter" region and the P type "base" region to the subsurface P+N+ junction and avoiding noise and electrical instability in the diode. In the described embodiment of the invention, after a first opening for determining the lateral extent of the P type "base" region (and other base regions in the integrated circuit being made) has been formed in a first overlying oxide layer, a first layer of resist is formed on the surface of the integrated circuit, and a second opening is formed therein for determining the lateral extent of the P+ subsurface region. A heavy dose of P type ions is implanted in the surface of the portion of the first N type region through the second opening in the resist, the resist functioning as a mask against the ions. The resist is then removed, exposing the silicon surface through the first opening. A "predeposition" layer of P type ions is formed in the exposed silicon surface either by a lighter concentration ion implantation step or other conventional diffusion process, with the surrounding oxide layer functioning as a mask. A "drive-in" diffusion step is performed by heating the integrated circuit to a predetermined high first temperature for a first predetermined time to diffuse the P type "base" region into the first isolated N+ type region.

In the above described embodiment of the invention, the predetermined first temperature and the first predetermined time are those selected for a predetermined "conventional" bipolar integrated circuit manufacturing operation to produce predetermined transistor characteristics and/or other device characteristics (such as diffused resistor characteristics).

After the "drive-in" diffusion step has been performed, the resulting structure then includes a heavy doped P+ implanted region extending from the surface of the integrated circuit into a first N type isolated region. The heavily doped P+ region is laterally surrounded by and contiguous with a much more lightly doped P type base region. The heavily doped P+ type implanted region then extends slightly below the bottom of the surrounding portions of the P type region (due to the much higher concentration of P type impurities in the P+ implanted region than in the surrounding P type region).

A second layer of oxide is then formed on the integrated circuit and a third opening is formed therein for determining the lateral extent of the N+ type "emitter" region. The third opening subtends and surrounds, the P+ type implanted region. An N+ diffusion step then is performed, forming the very heavily doped N+ type "emitter" region. The N+ impurity concentration is substantially higher than the P+ impurity concentration of the P+ type implanted region, and therefore converts the upper portion of that region to N+ type material, the lower portion of the P+ type implanted region remaining P+ type and constituting the above-mentioned "P+ type subsurface region". The electrical characteristics of transistors formed elsewhere in the integrated circuit are substantially unchanged by the process modifications needed to form the P+ subsurface region in the first N type region. The very high P+ and N+ impurity concentrations on either side of the P+N+ subsurface junction between the N+ type "emitter" region and the P+ type subsurface region result in a very low avalanche (or zener) voltage, as desired.

Embodiments of the present invention will now be described with reference to the accompanying drawings, in which:

Fig. 1 is a partial perspective section view of an integrated circuit structure after an isolation diffusion therein has been completed and an oxide opening has been made defining the lateral extent of the base region;

Fig. 2 is a partial perspective section view illustrating the structure shown in Fig. 1 after and for explaining further processing steps in the manufacture of the subsurface avalanche diode according to an embodiment of the present invention;

Fig. 3 is a partial perspective section view for use in explaining a further processing step of the structure shown in Fig. 2;

Fig. 4 is a partial perspective section view of the structure shown in Fig. 3 after the performing of further processing steps;

Fig. 5 is a partial perspective section view illustrating the structure shown in Fig. 4 after the subsurface avalanche diode of an embodiment of the invention has been formed therein, and

Fig. 6 is a partial perspective section view of a prior art structure, for use in pointing out the distinguishing features of the present invention.

The invention can perhaps be best understood by first describing the structure of an embodiment of a completed subsurface avalanche diode with

reference to Fig. 5. Fig. 5 is a partial perspective section view of an integrated circuit structure after completion of the last major operation in the manufacturing process, which is described below. Note that the steps of cutting oxide openings and providing metalized connections to the anode and cathode of the subsurface avalanche diode 20 in Fig. 5 have been omitted for simplicity. These steps are completely conventional in the integrated circuit manufacturing art and do not form part of the invention.

Referring to Fig. 5, integrated circuit structure 10 includes a lightly doped P type substrate 5, which typically may be approximately 15 mils thick. A relatively lightly doped N type epitaxial layer 3 is disposed on the upper surface of substrate 5. A plurality of heavily doped P type isolation diffusion regions 1 extending from the upper surface of N type layer 3 to P type substrate 5, from a plurality of electrically isolated N type regions such as 3A. (It should be appreciated that various vertical NPN transistors, lateral PNP transistors, and diffused resistors can be formed in the various isolated N type regions other than the one shown in Fig. 5. Such isolated N type regions are hereinafter referred to as "collector" regions. Most often, however, heavily doped N+ regions, commonly referred to as "emitter" regions, are diffused into P type "base" regions to form the emitters of vertical NPN transistors. All of the above recited structure is entirely conventional in the bi-polar integrated circuit technology).

The subsurface avalanche diode generally designated by reference numeral 20 in Fig. 5 is provided in an N type isolated region 3A. Subsurface diode 20 has a P+N+ junction 29 which exists entirely beneath the upper surface 3' of the N type layer 3. The cathode of subsurface avalanche diode 20 includes a heavily doped N+ peripheral region 27', which as will be explained below, is a portion of the overall N+ "emitter" region 27. Peripheral region 27' is contiguous with and completely laterally surrounds an inner portion 27'' of emitter region 27. Subsurface avalanche diode 20 includes a heavily doped P+ subsurface region 19'' that is included in and can be considered a part of the P type "base" region generally designated by reference numeral 18 in Fig. 5. (It should be appreciated that P type region 18 is being referred to herein as a "base" region simply because it is formed during the P type diffusion step that is also used to form all of the transistor P type base regions elsewhere in the integrated circuit structure. Similarly, the N+ region designated by reference numeral 27 is being referred to herein as an "emitter" region simply because N+ region 27 is formed during the same diffusion step that produces the N+ emitters of the NPN transistors formed elsewhere in the integrated circuit structure. Since this terminology is commonly used in this manner by those skilled in the art, it will be readily understood as used herein.)

The concentration of N type impurity carriers in region 27'' is typically roughly 10^{20} atoms per cubic centimeter. The concentration of P+ impurities in region 19'' is typically in the range from 10^{19} to 10^{20} atoms per cubic centimeter; a typical value in region 19'' would be approximately 4×10^{19} atoms per cubic centimeter if it is desired that the avalanche or zener breakdown voltage of subsurface junction 29 is to be approximately 6.5 volts. Lower concentrations of P+ impurities in region 19'' adjacent to junction 29 would have the effect of increasing the avalanche breakdown voltage of subsurface avalanche diode 20.

In a typical integrated circuit manufacturing process, the sheet resistance of base region 18 might be from 150 to 250 ohms per square for a junction depth of approximately 1.5 microns, corresponding to P type impurity concentrations in the range from 7×10^{18} to 1×10^{19} atoms per cubic centimeter, respectively. Higher values of P type impurity concentrations in base region 18 would result in lower emitter region to base region avalanche or zener breakdown voltages. Normally, the emitter-base breakdown voltage would tend to occur at the surface points designated by reference numerals 31, and would be subject to the previously described instabilities. However, the presence of subsurface P+ region 19'', with its P type impurity concentration being substantially higher than that anywhere in regions 19A' of base region 18, including surface points 31, causes the breakdown voltage along P+N+ junction 29 to be substantially lower than that at surface points 31.

As will become more clear, the subsequently described embodiment of a manufacturing process of the present invention makes it possible for the avalanche breakdown voltage of subsurface P+N+ junction 29 to be substantially lower than is practical (without undue surface damage) for the prior art subsurface avalanche diode junctions such as 29' in Fig. 6, which shows the salient features of the most common prior art subsurface avalanche or zener diode structure.

Before explaining in detail the advantages of the subsurface avalanche or zener diode structure shown in Fig. 5 over the closest prior art, it will be helpful to understand first in detail the manufacturing process the structure shown in Fig. 5. This process will now be described with reference to Figs. 1—4 and differences between the manufacturing processes of embodiments of the present invention and of the prior art will be explained.

Referring now to Fig. 1, the integrated circuit structure 10 is shown after the P+ isolation diffusions 1 have been formed. The surface impurity concentration N_s for the process of diffusing P+ isolation diffusions 1 is a non-critical parameter in the process of the present invention, and typically lies anywhere in the range from 10^{19} to 10^{20} atoms per cubic centimeter. As in any deep P+ isolation diffusion, the concentration of P type carriers falls off rapidly from its initial surface value N_s. As those skilled in the art will

appreciate, the fact that this surface concentration is a non-critical manufacturing parameter reduces the cost of precisely controlling the manufacturing process over what it would be if N_s were a critical parameter, as is required for the above-mentioned prior art processes for making subsurface avalanche diodes.

In contrast, the corresponding P+ isolation diffusion steps required in previously mentioned U.S. Patents No. 4,213,806 and No. 4,127,859 require surface concentration N_s as high as approximately 3×10^{20} atoms per cubic centimeter in order to obtain an avalanche voltage even as low as 7 volts along a junction such as N+P+ junction 29' of the prior art structure shown in Fig. 6. Those skilled in the art know that such a high surface concentration for a boron diffusion (which is used to form the isolation region and base region in most conventional integrated circuit manufacturing processes) causes severe surface "pitting" problems which have plagued the integrated circuit industry for years. The foregoing high surface concentrations for the P+ isolation diffusions also induce severe dislocations in the silicon at surface 3'' of the N type epitaxial layer 3A in the prior art structure of Fig. 6. During a subsequent drive-in step during which the isolation regions 1' are diffused through the N type region to the P+ substrate, these dislocations propagate through the N type region 3A, causing the ultimately formed diode junctions 29', 35 and 37 of Fig. 6 to have highly undesirable leakage currents that are highly temperature dependent and cause undesired drift in the electrical characteristics of the ultimately formed subsurface avalanche junction diode. Consequently, it is rather undesirable to use the structure of Fig. 6 as a subsurface avalanche diode junction which has a breakdown voltage of much less than approximately 7 volts, due to the high level of surface damage and consequent lower yields and high instability.

Returning again to Fig. 1, after the isolation diffusions 1 have been formed, according to this embodiment of the manufacturing process of the present invention, an opening 7 is produced in the silicon dioxide layer 9 that has been formed on the upper surface 3' of N type epitaxial layer 3 to define the lateral extent of "base" region 18 (Fig. 5) by exposing area 13 on surface 3' of collector region 3A. Opening 7 is formed at the same time that the "base openings" (not shown) are formed for the NPN transistors formed elsewhere in the integrated structure.

Referring now to Fig. 2, the next step in the process of this embodiment is to deposit a layer of typical photoresist 11 (which can be approximately 1 micron thick) on the entire upper surface of the integrated circuit structure 10 to function as an ion implantation mask. Then, an opening 15 is produced in photoresist layer 11 centrally within the above-mentioned "base opening" 7 to expose an area 13' of surface 3'. Then, using standard ion implantation apparatus and procedures, a P+ region 18 is implanted into the surface 13' through opening 15, as indicated by arrow 17, which represent bombardment of the entire upper surface by boron atoms, thereby forming the P+ region designated by reference numeral 19 in Fig. 2. In the described embodiment of the invention, wherein it is desired to obtain an avalanche breakdown voltage of approximately 6.5 volts in the ultimately formed subsurface avalanche junction 29 (Fig. 5), the surface concentration of region 19 is approximately 4×10^{19} atoms per cubic centimeter. The ion energies used are approximately 50 kev. However, the impurity concentrations of region 19 can be in the range from 1×10^{19} to 1×10^{20} atoms per cubic centimeter.

Referring now to Fig. 3, the next step in the manufacturing process is to remove photoresist layer 11, thereby exposing the entire surface area 13 through oxide opening 7. Surface area 13', of course, also remains exposed. Then, as indicated by arrows 21, the integrated circuit structure 10 is again bombarded by boron ions, implanting a P type region 19A into the exposed portion of surface 13 surrounding P+ region 19. The surface concentration of the region 19A depends on the desired resistivity or sheet resistance of the base regions of vertical NPN transistors being formed elsewhere in the integrated circuit, and can vary typically from approximately 7×10^{18} to 1×10^{19} atoms per cubic centimeter. This ion bombardment increases the P type impurity concentration in region 19A somewhat, but has little relative affect on the already very high doping level in region 19.

Referring now to Fig. 4, the next step in the manufacturing process is to subject the integrated circuit structure 10 to an elevated temperature (typically 1100 degrees centigrade) for a sufficiently long time (typically 2 hours) to "drive in" regions 19 and 19A, thereby producing relatively deep regions 19' and 19A' as shown in Fig. 4. At the same time that regions 19A' are formed, the base regions of vertical NPN transistors elsewhere in the integrated circuit structure also are formed. The depth of regions 19A' are approximately 2.5 microns in the described embodiment of the invention.

Referring now to Fig. 5, the next steps in the process are to form a thermal oxide layer 23 over the exposed silicon surface area, etch an "emitter opening" 25 therein, and diffuse in an N+ "emitter" region 27. The oxide opening 25 completely surrounds and is spaced from the intersection 33 of region 19' with the upper surface 3'.

Thus, the emitter region 27 includes a peripheral portion 27', which has a surface concentration of approximately 10^{20} atoms per cubic centimeter, and an inner portion 27'', which has a somewhat lower "net" N type impurity concentration, since the P type impurity concentration in this region was initially much

higher than in the remaining portions of base region 18. The lower impurity concentrations in N+ region 27'' in Fig. 5 typically may be of the order of 7×10^{19} atoms per cubic centimeter.

With the foregoing background, those skilled in the art will readily recognize that in the foregoing manufacturing process, the amount of time during which the high temperature to which the integrated circuit structure 10 is submitted after P+ region 19' (Fig. 4) is formed is not considered to be very great. This is because the emitter diffusion forming emitter region 27 does not require sufficiently high temperatures for sufficiently long periods of time to cause many of the P type impurities in region 19' to diffuse significantly deeper into N type region 3A toward substrate 5.

In contrast, however, in the prior art manufacturing processes, if a sufficiently low surface impurity concentration is used in forming P+ isolation regions 1' (Fig. 6) to avoid unacceptable severe surface damage, pitting, etc. and dislocation formation in the silicon, then the diffusion profile of isolation regions 1' will have fallen off so sharply that the P+ impurity concentration along the prior art subsurface junction 29' (Fig. 6) will inevitably be substantially lower than is the case along subsurface junction 29 of the embodiment of the subsurface avalanche diode 20 shown in Fig. 5. Thus, it will be appreciated that the above-described process inherently has the capability of making subsurface, highly stable, lower voltage avalanche or zener diodes than has been previously possible.

Those skilled in the art will now fully appreciate that in order to control the breakdown voltage of subsurface avalanche diode 29' of the prior art structure shown in Fig. 6, it will be necessary to place very "tight control" on the various diffusion process parameters used to form isolation junctions 1', thereby adding both cost and inconvenience to a manufacturing step that is usually considered to be noncritical.

Another severe shortcoming of the prior art structure shown in Fig. 6 will now be discussed. Upon inspection of Fig. 6, it can be seen that the subsurface N+P+ junction 29' inherently has in parallel therewith the "sidewall" junction areas designated by reference numerals 35, which constitute a P+N+ junction, and also the P+N+ junction area represented by reference numeral 37 in Fig. 6. Those skilled in the art will appreciate that in order to prevent the anode of the subsurface diode shown in Fig. 6 from being shorted to the P type substrate 5', an N+ buried layer 39 must be formed therein. These additional PN junctions represent two "parasitic" subsurface diodes that are connected in parallel with the desired low voltage subsurface avalanche junction 29'. There junction capacitances, the sums of which are more than double the junction capacitance of junction 29', greatly increase the total capacitance of the resulting avalanche diode. Furthermore, any leakage currents associated with these parasitic junctions add to the leakage current of the junction 29'. As previously mentioned, in some circuit applications requiring precise, low voltage, stable avalanche reference diodes, this high capacitance would be highly undesirable. Any additional leakage current contributed to that of subsurface junction 29' of the prior art device of Fig. 6 is highly undesirable, since it is heavily temperature-dependent, and increases the instability of the subsurface diode. Furthermore, it should be appreciated that the additional parasitic junction area inherent in the structure of Fig. 6 increases the susceptibility of the avalanche diode to the harmful effects of the thermally propagated dislocations that initially occur at the silicon surface as a result of the above-mentioned heavy surface dopant concentrations required for the P+ diffusions to produce regions 1'.

It should be appreciated that for a typical boron diffusion predeposition step, the initial surface concentration of dopant from the predeposition source must be very high. The actual diffusion profile of the completed junction is such that the P+ impurity concentration of the isolation region is much lower at the depth of the emitter diffusion junction than would be the case if the P+ isolation diffusion regions 1' of Fig. 6 did not need to be so deep.

The subsurface avalanche diode structure shown in Fig. 5, and the process for making that structure overcome the shortcomings of the prior art structures by avoiding the above-described parasitic junction capacitance and parasitic junction leakage currents. In the integrated circuit structure 10 of Fig. 5, no parasitic junctions (such as 35 and 37 of Fig. 6) are present. The absence of thermally propagated dislocations in the silicon crystal structure and absence of extensive "parasitic" junction area results in high yields (and thus lower product costs) and "harder" (i.e., more leakage-free) junctions for reference diodes than is the case of the prior art structures. The structure of the present invention also avoids the need for making the P+ isolation regions 1 with a "critical" or "tightly controlled" diffusion process, thereby allowing relaxation of the control of that stage of the process and thereby reducing the cost thereof. The process described for making the structure of Fig. 5 does not require any high temperatures additional to those already present in the most conventional bipolar integrated circuit processes in order to "anneal out" the amorphous silicon produced by the initial implantation of regions 19 (Fig. 2), because this annealing is automatically accomplished during the normal high temperature base diffusion step and emitter diffusion step. Therefore, this makes it easy for the process engineers to adjust slightly the emitter diffusion cycle to obtain desired values of bipolar transistor gain (i.e., "beta") as is the common practice. This later step would be very difficult if a subsequent high temperature annealing step were required, as is the case for the previously mentioned prior art process step

including implanting a subsurface P type region after the emitter regions have been formed.

While the invention has been described with reference to a particular embodiment thereof, those skilled in the art will be able to make various modifications to the disclosed structure and method without departing from the true spirit and scope thereof. It is intended that all substantial equivalents of the described steps and elements of the described process and structure, respectively, which achieve substantially the same results of obtaining low subsurface avalanche or zener breakdown voltages with low parasitic junction capacitance and low parasitic leakage currents in substantially the same way without causing excessive surface damage to the semiconductor surface be encompassed by the present invention. For example, it is not critical that any particular step for providing a doped region include an ion implantation step or convection thermal deposition step. Similarly, it is not essential to the concept that any particular masking material be used, as long as it accomplishes the masking function. For example, if controlled ion beams are used, no mask at all would be needed. Although rectangular regions are shown for convenience of illustration, round geometry for regions 19'' and 27'' might preferably be provided to avoid localized field concentrations and preferential breakdown sites.

Claims

1. A low voltage integrated circuit subsurface avalanche or zener diode comprising in combination:

a p type substrate having a first surface;
an N type layer on said first surface, said N type layer having an outer surface;
a P+ isolation region extending from said outer surface through said N type layer to said P type substrate to isolate electrically a first N type region of said N type layer from any other portion thereof;
a P type region disposed in said first N type region, the junction between said P type region and said N type region terminating at said outer surface;
a heavily doped N+ region disposed in said P type region, the junction between said P type region and said N+ region terminating at said outer surface, and
an entirely subsurface P+ region continuous with and laterally surrounded by said P type region and disposed beneath and contiguous with said N+ region and forming a subsurface P+N+ junction therewith;
the majority carrier impurity concentration on each side of said subsurface P+N+ junction greatly exceeding the P type impurity concentration at any point along the boundary between said P type region and the peripheral portion of said N+ region.

2. A diode according to Claim 1 wherein said N+ region includes an annular peripheral portion that extends laterally outwardly beyond all peripheral portions of said subsurface P+ region.

3. A diode according to Claim 1 or 2, wherein the thickness of said N type layer is in the range from approximately 6 microns to 8 microns.

4. A diode according to any preceding claim wherein the impurity concentration of said subsurface P+ region is in the range from 1×10^{19} to 1×10^{20} atoms per cubic centimeter.

5. A diode according to any preceding claim wherein the impurity concentration of said N+ region is approximately 1×10^{20} atoms per cubic centimeter.

6. A diode according to any preceding claim wherein the bottom of said subsurface P+ region is located a substantial distance from the bottom of said N type layer.

7. A diode according to any preceding claim including an inner portion of said N+ region that is laterally coterminous with said subsurface P+ region and has less net N type doping than the peripheral portion of said N+ region.

8. A diode according to any preceding claim wherein the doping level and depth of said P type region are equal to the doping levels and depths of base regions of NPN transistors in another portion of said N type layer.

9. A diode according to any preceding claim wherein the depth of said P+ isolation region is at least 8 microns and the surface impurity concentration of said P+ isolation region is less than approximately 1×10^{20} atoms per cubic centimeter.

10. A low voltage integrated circuit, subsurface avalanche or zener diode substantially as herein described with reference to Figure 5 with or without reference to any of Figures 1 to 4 of the accompanying drawings.

11. A process for making a low voltage integrated circuit subsurface avalanche or zener diode, said method comprising the steps of:

(a) forming a first opening in a first oxide layer on the surface of a semiconductor chip which includes a P type substrate and a plurality of electrically isolated N type regions disposed on said substrate, a plurality of P+ isolation regions extending from outer surfaces of said N type regions to said P type substrate, said first oxide layer being disposed on said outer surfaces, said first opening exposing a first area of the surface of a first one of said N type regions;

(b) exposing a second area of the surface of said first N type region, the boundary of said second area being spaced from and disposed entirely within the boundary of said first area;

(c) passing P type impurities through said second opening into the exposed second area of the surface of said first N type region to form a shallow, heavily doped P+ type first region that is coextensive with said second opening;

(d) passing P type impurities through said first opening to form a shallow P type second region surrounding and contiguous with said first region, said first region being substantially more heavily doped than said second region;

(e) heating said chip to diffuse said first and second regions deeper into said first N type region;

(f) forming a second oxide layer covering said first surface area and forming a third opening in said second oxide layer exposing a third area of the surface of said first N type region, the boundary of said third area being everywhere spaced from and disposed between the boundaries of said first and second areas;

(g) passing N type impurities through said third opening to form an N+ region in the exposed portions of said first region and said P type second region,

said N+ region having an inner portion approximately laterally co-extensive with said first region and a depth that is less than the depth of said first region, the bottom portion of said first region remaining P+ type, said N+ region also having a peripheral portion having an inner boundary that is essentially coterminous with an outer boundary of the junction between said P+ bottom portion of said first region, and said inner portion of said N+ region and said P+ bottom portion of said first region forming a P+N+ subsurface junction therebetween, the majority carrier impurity concentrations on each side of said P+N+ subsurface junction greatly exceeding the P type impurity concentration along the junction between said second region and said peripheral portion of said N+ region, thereby confining avalanching or zener tunnelling of the diode formed by said N+ region and said first and second regions to the vicinity of said P+N+ subsurface junction.

12. A process according to Claim 11 wherein step (d) includes bombarding said chip with ions.

13. A process according to Claim 11 or 12 wherein the P type ions of step (c) have energies in the range of from 30 to 70 kev.

14. A process for making a low voltage integrated circuit subsurface avalanche or zener diode, said method comprising the steps of:

(a) forming a first opening in a first oxide layer on the surface of a semiconductor chip which includes a P type substrate and a plurality of electrically isolated N type regions disposed on said substrate, a plurality of P+ isolation regions extending from outer surfaces of said N type regions to said P type substrate, said first oxide layer being disposed on said outer surfaces, said first opening exposing a first area of the surface of a first one of said N type regions;

(b) forming a layer of masking material on the outer surface of said first oxide layer, said layer masking material covering said first area of the surface of said first N type region;

(c) forming a second opening in said layer of masking material, exposing a second area of the surface of said first N type region, the boundary of said second area being spaced from and disposed entirely within the boundary of said first area;

(d) passing P type impurities through said second opening into the exposed second area of the surface of said first N type region to form a shallow, heavily doped P+ type first region that is coextensive with said second opening;

(e) removing said layer of masking material;

(f) passing P type impurities through said first opening to form a shallow P type second region surrounding and contiguous with said first region, said first region being substantially more heavily doped than said second region;

(g) heating said chip to diffuse said first and second regions deeper into said first N type region;

(h) forming a second oxide layer covering said first surface area and forming a third opening in said second oxide layer exposing a third area of the surface of said first N type region, the boundary of said third area being everywhere spaced from and disposed between the boundaries of said first and second areas;

(i) passing N type impurities through said third opening to form an N+ region in the exposed portions of said first region and said P type second region,

said N+ region having an inner portion approximately laterally co-extensive with said first region and a depth that is less than the depth of said first region, the bottom portion of said first region remaining P+ type, said N+ region also having a peripheral portion having an inner boundary that is essentially coterminous with an outer boundary of the junction between said P+ bottom portion of said first region, and said inner portion of said N+ region and said P+ bottom portion of said first region forming a P+N+ subsurface junction therebetween, the majority carrier impurity concentrations on each side of said P+N+ subsurface junction greatly exceeding the P type impurity concentration along the junction between said second region and said peripheral portion of said N+ region, thereby confining avalanching or zener tunnelling of the diode formed by said N+ region and said first and second regions to the vicinity of said P+N+ subsurface junction.

15. A process according to Claim 14 wherein said masking material is photoresist material.

16. A process according to Claim 14 or 15 wherein step (f) includes bombarding said chip with ions.

17. A process according to any of Claims 14 to 16 wherein the P type ions of step (d) have energies in the range from 30 to 70 kev.

18. A process according to any of Claims 11 to 17 including forming base regions for NPN transistors in other ones of said electrically isolated N type regions simultaneously with the forming of said second region and forming emitter regions for said NPN transistors simultaneously with the forming of said N+ region.

19. A process for making a low voltage integrated circuit subsurface avalanche or zener diode substantially as herein described with reference to Figures 1 to 5 of the accompanying drawings.

20. A highly stable low voltage integrated

circuit subsurface avalanche or zener diode made by the process of:

(a) forming a first opening in a first oxide layer on the surface of a semiconductor chip which includes a P type substrate and a plurality of electrically isolated N type regions disposed on said substrate, a plurality of P+ isolation regions extending from outer surfaces of said N type regions to said P type substrate, said first oxide layer being disposed on said outer surfaces, said first opening exposing a first area of the surface of a first one of said N type regions;

(b) forming a layer of masking material on the outer surface of said first oxide layer, said layer masking material covering said first area of the surface of said first N type region;

(c) forming a second opening in said layer of masking material, exposing a second area of the surface of said first N type region, the boundary of said second area being spaced from and disposed entirely within the boundary of said first area;

(d) bombarding the surface of said chip with P type ions, some of which pass through said second opening and are implanted in the exposed second area of the surface of said first N type region to form a shallow, heavily doped P+ type first region that is coextensive with said second opening;

(e) removing said layer of masking material;

(f) passing P type impurities through said first opening to form a shallow P type second region surrounding and contiguous with said first region, said first region being substantially more heavily doped than said second region;

(g) heating said chip to diffuse said first and second regions deeper into said first N type region;

(h) forming a second oxide layer covering said first surface area and forming a third opening in said second oxide layer exposing a third area of the surface of said first N type region, the boundary of said third area being everywhere spaced from and disposed between the boundaries of said first and second areas;

(i) passing N type impurities through said third opening to form an N+ region in the exposed portions of said first region and said P type second region,

said N+ region having an inner portion approximately laterally co-extensive with said first region and a depth that is less than the depth of said first region, the bottom portion of said first region remaining P+ type, said N+ region also having peripheral portion having an inner boundary that is essentially coterminous with an outer boundary of the junction between said P+ bottom portion of said first region, and said inner portion of said N+ region and said P+ bottom portion of said first region forming a P+N+ subsurface junction therebetween, the majority carrier impurity concentrations on each side of said P+N+ subsurface junction greatly exceeding the P type impurity concentration along the junction between said second region, and said peripheral portion of said N+ region, thereby confining avalanching of the diode formed by said N+ region, and said first and second regions to the vicinity of said P+N+ subsurface junction.

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